

TARGET188EB

Technical Manual

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Revision History

Manual	PCB	Comments	
Issue A	V1 I1	961107	First Release of Manual
Issue B	V1 I1	961218	Edits to Appendix F. Circuit Diagrams.
Issue C	V1 I1	981119	[ECO2717 & ECO2784]
Issue D	V1 I1	000411	[ECO2872]

Preface

The Manual

This manual details the operation and features of Arcom's TARGET188EB boards. It has been designed as both a guide to getting started with the TARGET188EB Development Kit and a reference for the hardware features of the board.

Name Conventions

Throughout this document an asterisk "*" suffix to a signal name denotes that a signal is active low (e.g. DATAACK*).

All numbers are in decimal unless otherwise indicated. Where a number is suffixed by 'h' the value is in hexadecimal format.

Problem?

You will find comprehensive details of how to contact various specific departments on page 2 of this manual.

Contents - Packing List

In your TARGET188EB package you should have:

- A TARGET188EB in a sealed anti-static bag.
- A document titled 'TARGET188EB User Manual' (this document)
- A document titled '188EB Target Board Monitor'
- A document titled '188EB Target Processor Quickstart'
- A high density 3 1/2" floppy disk titled 'TARGET188EB Monitor Disk'
- A high density 3 1/2" floppy disk titled 'TARGET188EB Board Software Library'

If you have the TARGET188EB Development Kit package you should also have:

- An SVIF1 (SourceView Interface 1) Development Interface Module
- A CAB-SVIF1 Development Interface Cable
- A high density 3 1/2" floppy disk titled 'TARGET188EB SourceVIEW'
- A document titled 'TARGET188EB SourceVIEW'

Utility Disks

- A high density 3 1/2" floppy disk titled 'TARGET188EB Monitor Disk'
- A high density 3 1/2" floppy disk titled 'TARGET188EB Board Software Library'
- A high density 3 1/2" floppy disk titled 'TARGET188EB SourceVIEW' (Development Kit only)

Two utility disks are provided with the TARGET188EB. The first contains source and assembled code for the monitor software pre-installed on the board together with a utility to convert assembled code into Intel Hex format to allow code download to the board via the monitor. The second disk contains C library routines for setting up and controlling the board, for use in applications code together with a disk based TARGET188EB Board Software Library Manual.

The Development Kit contains a third disk with Arcom's SourceVIEW development and debugging environment for use with the TARGET188EB.

Anti-Static Handling

This board contains CMOS devices which could be damaged in the event of static electricity being discharged through them. At all times, please observe anti-static precautions when handling the board and always unpack and install it in an anti-static working area.

Electromagnetic Compatibility (EMC)

The TARGET188EB is classified as a 'component' with regard to the European Community EMC regulations and it is the user's responsibility to ensure that systems using the board are compliant with the appropriate EMC standards.

The TARGET188EB, when used in an Arcom CRATE3CE enclosure, are CE approved under Arcom's STEbus Technical Construction File.

Packaging

Please ensure that should a board need to be returned to Arcom, it is adequately packed. Use an anti-static bag for the board and use a box not bag to physically protect the board. Retain the original packing if possible.

Section 1. Introduction

TARGET188EB is a Eurocard sized target CPU board developed specifically for embedded applications offering the following features:

- Intel 188EB microprocessor running at 25MHz
- STEbus 8-bit expansion interface
- PC/104 8-bit expansion interface
- 128KB SRAM as standard, 256KB option available (8-bit wide access)
- 128KB socketed 5V Flash EPROM on-board as standard (8-bit wide) with resident monitor software
- Socket for further 32/64/128/256KB ROM which may be 5V Flash EPROM
- Programmable memory and I/O maps
- Two 120KBaud (max.) RS232 serial communications ports (one Zilog 85230 SCC)
- Watchdog timer
- One TTL 8-bit digital output port
- One TTL 8-bit digital input port
- One TTL 8-bit digital input/output port
- Flexible hardware interrupt support
- Software development/download port (SVIF1 port)
- Two user links
- Two user LEDs and +5V power LED

The TARGET188EB is available as four variants:

Variant Name	Specification
TARGET188EB	STEbus Master and PC/104 Master, 128K SRAM
TARGET188EB-H	STEbus Master and PC/104 Master, 256K SRAM
TARGET188EB-SBC	PC/104 Master only, 128K SRAM
TARGET188EB-SBC-H	PC/104 Master only, 256K SRAM

This manual covers all variants.

The TARGET188EB is shipped with a software monitor blown into a 128K Flash EPROM to allow simple exercising of the board and downloading application code.

The Development Kit contains an additional 128K Flash EPROM with the 'remote' target portion of Arcom's SourceVIEW development software blown into it. By using the board with the TARGET188EB Development Kit the user can develop and debug application software very quickly. See the SourceView manual for more details.

Section 2. Getting Started

This section is designed to familiarise the user with the features of the TARGET188EB and demonstrate the use of the monitor software. It assumes that you have the cables provided with the Development Kit.

Equipment required

- TARGET188EB Development Kit
- STEbus rack and backplane with power supply OR
- Power supply (+5V at 1A minimum) connected up to PL4 (see Appendix B. Connections)
- IBM PC/AT compatible computer running terminal emulation software

Installation & Monitor Startup

Refer to Target188EB Quickstart Manual for more comprehensive instructions with drawings.

1. Ensure that the links on the TARGET188EB board are in their default configurations (see Section 3. Links and Options).
2. From the TARGET188EB Development Kit take the CAB-SVIF1 cable and plug the 10 way ribbon cable connector into the SVIF1 PL2 header.
3. Plug PL1 of the SVIF1 into PL2 (software development/download port) on the TARGET188EB. The body of the SVIF1 should lie over the TARGET188EB.
4. Align the TARGET188EB into the STEbus rack until it mates with one of the backplane connectors.

OR

Wire the +5V power supply cable to pin 2 of the PL4 screw terminal block and the 0V cable to either pin 5 or pin 6 of the terminal block.

5. Plug the 9 way D-type connector marked channel B on the CAB-SVIF1 cable into one of the COM ports on the PC/AT computer.
6. Configure the terminal emulation software on the PC/AT for communications via the appropriate COM port at 19200 Baud with 8 data bits, no parity and 1 stop bit. Set the protocol to 'none'.
7. Turn on the STEbus rack OR power supply - the surface mount power indicator LED on the TARGET188EB will illuminate.
8. The terminal emulator will display the following (software version may vary):

```

====<< TARGMON188 TARGET MINI-MONITOR >>====
                Version 1.02
Copyright (C) Arcom Control Systems 1996

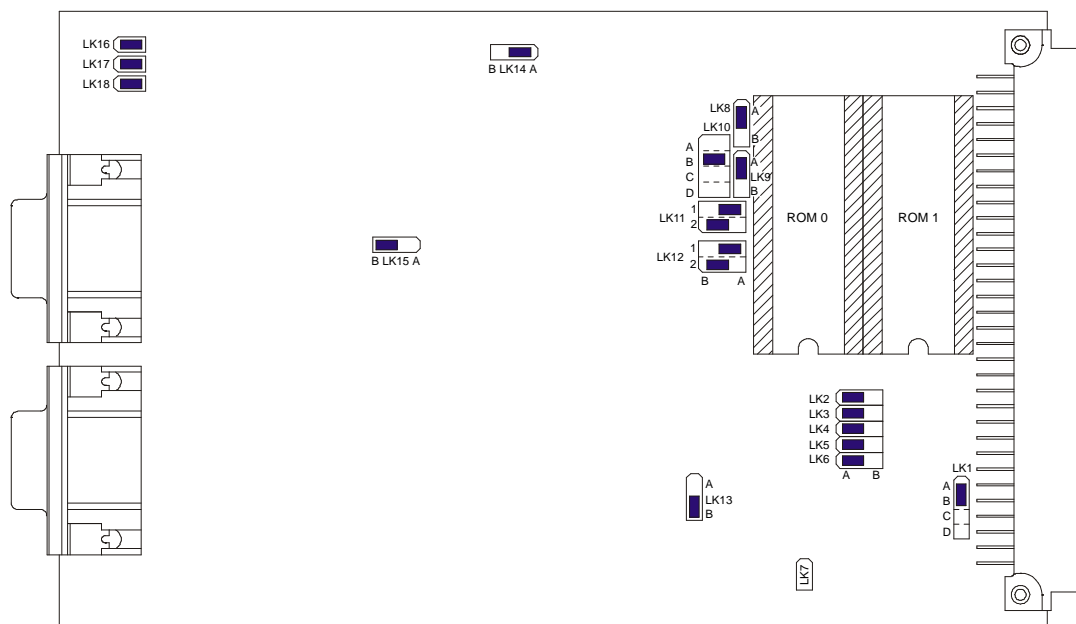
```

```
0100>
```

The monitor software is now running and can be used to exercise many areas of the board. The monitor also supports code download from a terminal emulator and Flash ROM programming. Press the 'H' key to display a command list. A full manual for operating the monitor is shipped with the TARGET188EB. 'Section 4. Using the TARGET188EB' describes the operation of the board in more detail and describes the tools available to develop applications code to run on the board.

Section 3. Links and Options

Default Link Positions



Note: A '+' next to a link position indicates the default shipping position.

LK1. STEbus SYSRST*

LK1	Function
+A	Board drives SYSRST* to backplane
B	Board receives SYSRST* from backplane
C	Board can be reset by push-button connected to PL3 only

LK2. INT3 source selection (1 link of 2)

LK2	Function
+A	PC/104 IRQ7 or STEbus TFRERR* (see LK13 also)
B	STEbus ATNRQ3*

LK3. INT2 source selection

LK3	Function
+A	PC/104 IRQ5
B	STEbus ATNRQ2*

LK4. INT0 source selection

LK4	Function
+A	PC/104 IRQ3
B	STEbus ATNRQ0*

LK5. NMI Source Selection

LK5	Function
+A	SIFI (SourceVIEW) Interface Port
B	STEbus TFRERR*

LK6. INT1 Source Selection

LK6	Function
+A	PC/104 IRQ4
B	STEBus ATNRQ1*

LK7. SRAM battery back-up from PL4

LK7	Function
+Omit	STEBus used - VSTBY from PL1
Fit	STEBus not used - VSTBY from PL4 pin 1

LK8. ROM1 write enable

LK8	Function
+A	Writes to ROM1 enabled
B	Writes to ROM1 disabled

LK9. ROM0 write enable

LK9	Function
+A	Writes to ROM0 enabled
B	Writes to ROM0 disabled

LK10. ROM size selection (ROM0 & ROM1) - see also LK11 & LK12

LK10	Function
A	256K EPROMs fitted
B	128K EPROMs fitted
C	64K EPROMs fitted
D	32K EPROMs fitted

LK11. ROM0 size selection - see also LK10 & LK12

LK11	1A	1B	2A	2B
EPROM size				
32K	omit	fit	omit	fit
64K	fit	omit	omit	fit
128K	fit	omit	omit	fit
256K	fit	omit	fit	omit

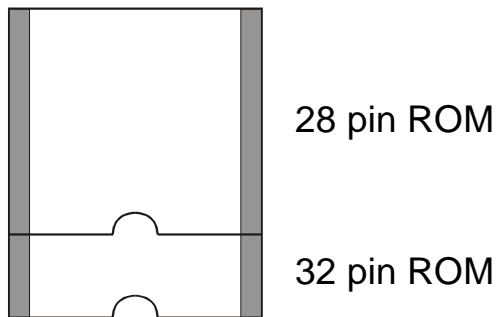
Note: Both EPROMs must be of the same size if the ROM address space is to be contiguous.

LK12. ROM1 size selection - see also LK10 & LK11

LK12	1A	1B	2A	2B
EPROM size				
32K	omit	fit	omit	fit
64K	fit	omit	omit	fit
128K	fit	omit	omit	fit
256K	fit	omit	fit	omit

Note: Both EPROMs must be of the same size if the ROM address space is to be contiguous.

ROM Fitting Guide



32 pin ROMs should take up the entire socket and should be fitted in the orientation shown in the 'Default Link Position' diagram.

28 pin ROMs should be fitted to only a portion of the socket, as shown above.

LK13. INT3 source selection (2 link of 2)

LK13	Function
+A	STEBus TFRERR*
B	PC/104 IRQ7

LK14. Watchdog source selection

LK14	Function
+A	Watchdog strobe driven from BCLK (i.e. disabled)
B	Watchdog strobe driven from 188EB port 2 bit 3 (i.e. enabled)

LK15. Timer 1 source selection

LK15	Function
A	Timer1 source driven from Timer0 out (cascade)
+B	Timer1 source driven from external source

LK16. Run Mode Select

Selects whether the processor runs the monitor software or the users application code after a power-up or reset. Application code must be set to start running at C0000H (lowest EPROM memory address).

LK16	Function
Omit	Run application starting at memory address C0000H
+Fit	Run monitor software

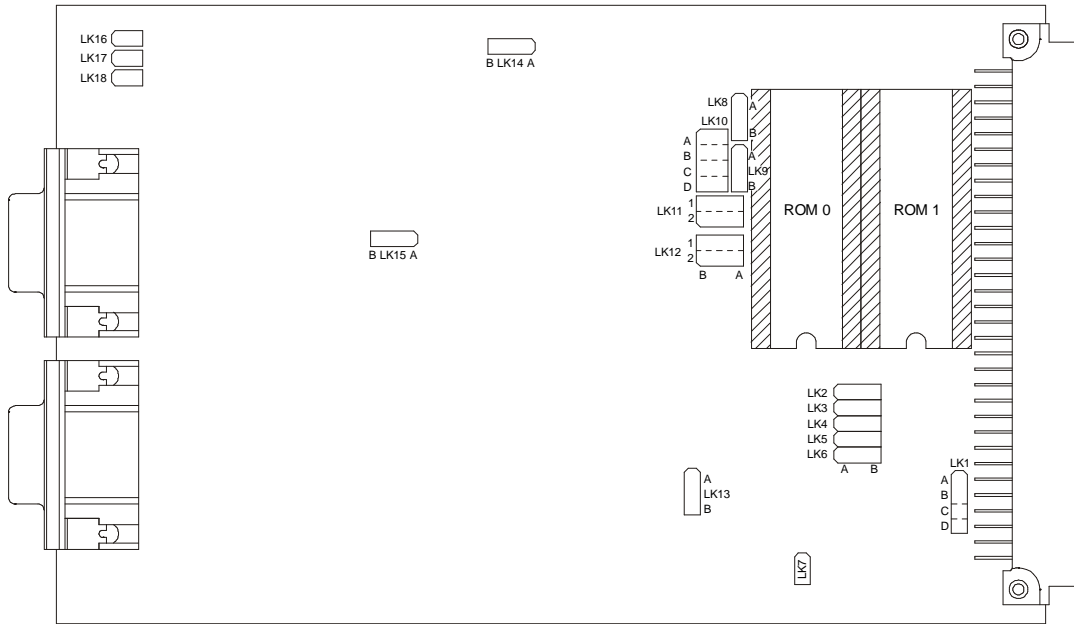
LK17. User Link 1. - CPU port P2 bit 4

LK17	Function
Omit	CPU port P2 bit 4 reads as 1
+Fit	CPU port P2 bit 4 reads as 0

LK18. User Link 2. CPU port P2 bit 5

LK18	Function
Omit	CPU port P2 bit 5 reads as 1
+Fit	CPU port P2 bit 5 reads as 0

User Configuration Record



Section 4. Using the TARGET188EB

Programmable Memory and I/O Map

The TARGET188EB has a very flexible scheme for locating its on-board memory, peripherals and expansion busses in its memory and I/O maps. The 188EB processor has eight outputs called 'general chip selects', GCS0 to GCS7. These outputs may be programmed so that they become active over a range of memory or I/O addresses and can be used to activate devices connected to the 188EB. The table below shows how the chip selects are used on the TARGET188EB with the default address ranges programmed by the monitor after initialisation.

188EB Chip Select	TARGET188EB Chip Select Use	Default Address Range
GCS7	Accesses STEbus	not programmed or enabled
GCS6	Accesses STEbus	not programmed or enabled
GCS5	Accesses STEbus	not programmed or enabled
GCS4	Accesses STEbus	not programmed or enabled
GCS3	Parallel Port	not programmed or enabled
GCS2	SVIF1 Port	FC0C-FC0F
GCS1	85C230 SCC Interrupt acknowledge	not programmed or enabled
GCS0	85C230 SCC	not programmed or enabled

Any CPU access to an address that is not covered by one of GCS0, GCS1, GCS2, GCS3, UCS (on-board ROM space) or LCS (on-board RAM) is automatically directed to the PC/104 bus. Boards using the STEbus can access peripheral boards on both PC/104 and STEbus. The STEbus is the non-default expansion bus. As shown in the table above, 188EB chip selects GCS4, GCS5, GCS6 and GCS7 can be used to direct CPU accesses that would normally go into the PC/104 bus to access the STEbus expansion bus instead.

This example illustrates the use of GCS3 to GCS6. The monitor software sets the TARGET188EB up so that the memory area from 20000h(128k RAM) or 40000h(256k RAM) to 7FFFFh is directed to the PC/104 bus by default. The user has an STEbus memory board that exists in the memory address range 60000h to 6FFFFh. Any one of GCS4 to GCS7 may be programmed to cover 60000h to 6FFFFh and CPU accesses to any address in this range will then be diverted to the STEbus instead of the PC/104.

GCS4, GCS5, GCS6 and GCS7 can be programmed very flexibly to create multiple 'holes' in the PC/104 memory or I/O space that are directed to the STEbus.

UCS and LCS are used to access on-board ROM and RAM respectively. The start address of UCS can be programmed to start anywhere from between 80000h and the top of UCS at FFFFFh, depending on the size of the ROM used. The LCS starts at memory address 00000h. The end address would normally be programmed to be 1FFFFh (for 128K SRAM) or 3FFFFh (for 256K SRAM).

The Board Software Library supplied with the development kit fully supports programming all the 188EB chip selects.

Programming the chip selects that control access to EPROM, memory and I/O can also be used to move these on-board peripherals around in the address map, see Appendix C. Reference for more details.

Memory Map

FFFFFh	16KB Monitor (UCS) after initialisation	
FC000h	Flash ROM0 (UCS)	
E0000h	Flash ROM1 (UCS) [optional]	
C0000h		
80000h	Max. ROM1 space (UCS)	STEBus or PC/104
7FFFFh	PC/104 or STEBus (GCS4-7)	
40000		
3FFFFh	Alternative 256K RAM (-H version) (LCS)	STEBus or PC/104
20000		
1FFFFh	128KB SRAM (LCS)	
0000h		

Memory Map After Power-up/Reset

After reset the upper chip select UCS is enabled with the top 1KB memory address space as its address block. This allows the boot monitor program to run from the top of memory. The UCS register is then programmed by the monitor software to assert the ROM chip selects at addresses from 80000h to FFFFFh (512KB).

The state of LK16 tells the monitor whether to run itself or the user's application code. Application code must always start running from address C0000h (bottom of ROM). Having the ROM occupy this much of the memory map may obscure areas of the memory map required by PC/104 or STEBus peripheral boards. If this is the case then the application code can be written to re-program the start address of UCS while it is running to effectively limit the size of the ROM. Code should be written to jump into the reduced ROM area and then to re-program UCS for the new size. If only one 128K ROM is used code should be written to jump to a starting address of E0000h. Memory space between the bottom of ROM and the top of main RAM (location selected by LCS) will be automatically mapped to the PC/104 bus. GCS4-7 can be programmed to direct accesses to the STEBus.

Note: when running the monitor software on 256KB RAM variants of board the extra 128KB of RAM is not accessible until chip select LCS is re-programmed.

I/O Map

FFFFh	PC/104 or STEbus (GCS4-7)
FC0Fh	
FC0Ch	
F8FFh	
F000h EFFFh	
0000h	PC/104 STEbus (GCS4-7)

On-Board Control Registers

SVIF1 Port Registers

The SVIF1 port takes up 4 bytes of I/O space.

The default base address of the SVIF1 port under the monitor software is I/O FC0Ch.

A1	A0	Function
1	1	Channel A Data
1	0	Channel B Data
0	1	Channel A Control
0	0	Channel B Control

Bus Timeout Clear

A read from the I/O address range setup for chip select GCS3 (parallel port) will clear a bus timeout when address lines A0 and A1 are high.

User Links and LEDS

The TARGET188EB has two user links and two user LEDs and a link that determines whether the monitor software or application code is run on power-up or reset. These links and LEDs are connected directly to the 188EB processors integral parallel port pins as follows:

Links

Reference	188EB Parallel Port Connection
LK16	Port P2 bit 2 (this link is used for run mode selection by the monitor)
LK17	Port P2 bit 4
LK18	Port P2 bit 5

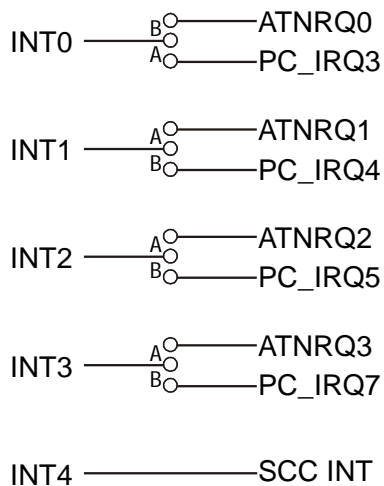
LEDs

Reference	188EB Parallel Port Connection
D2 (red)	Port P2 bit 7
D3 (green)	Port P2 bit 6

The C library routines supplied with the TARGET188EB fully support the configuration of and access to these peripherals.

Interrupt Assignments

Interrupts from STEbus, PC/104 and on-board peripherals are routed to the 188EB INT4-0 lines via links for ease of configuration. The link arrangement is shown below.



STEbus interrupts are level triggered, 188EB on-board peripherals can be configured to use edge- or level triggered interrupts.

Note that the board can only receive interrupts on STEbus ATNRQ0, ATNRQ1*, ATNRQ2* or ATNRQ3*. ATNRQ4-7* are not connected to the board.*

Parallel I/O port

To use this onboard facility it is necessary to program GCS3 for the address range that the user wishes to site the parallel I/O port.

There are three TTL 8-bit digital I/O ports covered by this chip select.

- 1 digital I/O port
- 1 digital input port
- 1 digital output port

To access the output port A1 and A0 must be '0'.

To access the input port A1 is a '0' A0 is a '1'.

To access the I/O port A1 is a '1' A0 is a '0'.

If a read occurs from the I/O address range set in GCS3 and A1 and A0 are '1' this will clear a bus time-out.

When using the I/O port as an input port firstly set the outputs to '1'.

STEBus Support

The TARGET188EB is compliant with the STEbus IEEE1000 specification.

PC/104 Support

The TARGET188EB is compliant with version 2.3 of the PC/104 specification. It supports memory and I/O reads and writes as a sole master to 8 bit PC/104 peripheral boards. It does not support DMA or other PC/104 masters in the same module stack.

Battery Back-up

The TARGET188EB supports battery backup of its main system SRAM via the +VSTBY line on the STEbus or via pin 1 of the power connector PL4.

Using the STEbus, a +3.6V (or similar) source should be connected between +VSTBY (+ve terminal) and GND (-ve terminal) on the STEbus backplane.

Using the board as an SBC, a +3.6V (or similar) source should be connected between pin 1 (+ve terminal) and pin 6 (-ve terminal) of PL4.

Battery backup current is approximately 5 μ A.

Watchdog

The TARGET188EB has a watchdog time-out facility fixed at 1200ms. If no strobe is received by the watchdog circuit for 1200ms then a CPU reset is generated. LK14 selects the watchdog strobe source. A link in position A (factory default) selects BCLK as the watchdog source; i.e. watchdog is disabled. Position B selects the 80188EB port 2 bit 3 as the watchdog source. If the link is set to position B, the user application code must ensure that port 2 bit 3 is toggled with a period of less than 1200ms.

Utility Disks

The TARGET188EB Monitor Disk contains four files:

TMON188.C	Source code for monitor software
TMON188.BIN	Assembled code for monitor software
BIN2HEX.EXE	Utility to convert binary files to Intel Hex format to enable them to be downloaded using on-board monitor.
TMON188.EPR	.EPR file for 27C010

The operating manual for the monitor software is shipped with the Development Kit.

The Next Step

The monitor software installed allows the user to become familiar with the board's basic features. Arcom supplies a number of options to aid the user in developing application code to fully utilise the TARGET188EB's facilities.

A board utility library written in C is supplied with the Development Kit. This contains routines that allow application code to easily set up and control on board peripherals such as the interrupt controller, CPU programmable chip selects, serial communications channels, watchdog timer, counter/timers, user links and LEDs. For users who do not wish to use these routines Appendix D. Bibliography lists the datasheets for the on-board peripherals.

SourceVIEW, a low cost solution to code development and debugging for the TARGET188EB is shipped with the TARGET188EB Development Kit. The board is shipped with the 'remote' target portion of the system blown into a flash EPROM at board address C0000H. This runs if LK16 jumper is removed before power-on/reset. With the host portion of the SourceVIEW system running on a PC/AT compatible a complete source level debugging environment can quickly be constructed. See the SourceView manual supplied with the Development Kit for more details.

Arcom can supply a range of other tools for source level development and debugging as well as real time operating systems and development tools. Please contact Arcom for details.

Section 5. Troubleshooting

Problem	Suggestions
<ul style="list-style-type: none"> No sign-on screen on terminal when running with SVIF1 	<ul style="list-style-type: none"> Check power-on board - red surface mount LED should be lit. Check baud rate, stop bits and parity of terminal. Check links in default positions especially LK16 (should be fitted). Check connections to correct COM port.
<ul style="list-style-type: none"> Can't access STEbus peripheral board 	<ul style="list-style-type: none"> Check that SYSRST* is being driven on power-up by one board only in the system Check that SYSCLK is being driven by one board in the system. Check that STEbus address range being accessed is available off-board (is it covered by one of the on-board memory or general chip selects). Check that at least one general chip select GCS4-7 has been set up to cover the required address range.
<ul style="list-style-type: none"> Can't access PC/104 peripheral board 	<ul style="list-style-type: none"> Is the address range being accessed available to the PC/104 bus? Ensure that it is not covered by one of the general chip selects (GCS0-7). Is the PC/104 board correctly plugged onto the target board?

Appendix A. Specification

Microprocessor	Intel 80188EB
Speed	25MHz
Memory	Sockets to hold up to 512KB ROM (8-bits wide, two wait states) top 16KB occupied by monitor software. 5V Flash EPROMs may be programmed on-board. 128KB or 256KB main system SRAM (8-bits wide, one wait state)
Peripherals	1 x 85230 SCC RS232 serial communications ports (120KBaud max.) with RX, TX, CTS, RTS, DSR, DTR, DCD and RI Arcom SVIF debug/development port Watchdog timer fixed at 1200ms generates CPU reset (link selectable) 3 counter/timers. Each counter can generate an interrupt on a shared interrupt line 24 bit parallel I/O port Two user LEDs Two user links plus run monitor/run application link Power monitor generates CPU reset if +5V supply drops below 4.62V +/- 0.12V. Reset button connector
Expansion	STEBus IEEE1000 compatible master mode PC/104 version 2.3 compatible, 8 bit only. DMA and MASTER* modes not supported
Temperature	Operating: 0 to 55°C Storage: 0 to 70°C
Humidity	10% to 80% RH (non-condensing)
Power	+5V @ 810mA typical +12V and -12V routed to PL1, PL4, PL6 and PL7 but not used on board
Battery Backup	External +3.6v@ 5µA
Dimensions	160mm x 100mm
Weight	140g (TARGET188EB) 160g with 2x 128k EPROMs fitted
MTBF	320000 hours

Appendix B. Connections

PL1. STEbus Connector

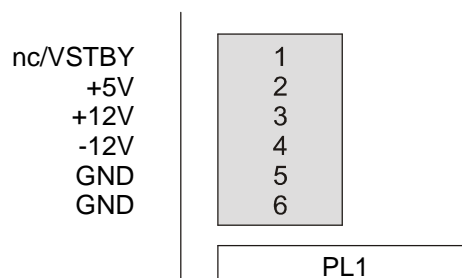
Standard 64way a&c row DIN41612 right angle PCB mount plug. Pin-out in accordance with IEEE1000 specification.

PL1

GND	a1	c1	GND
+5V	a2	c2	+5V
D0	a3	c3	D1
D2	a4	c4	D3
D4	a5	c5	D5
D6	a6	c6	D7
A0	a7	c7	GND
A2	a8	c8	A1
A4	a9	c9	A3
A6	a10	c10	A5
A8	a11	c11	A7
A10	a12	c12	A9
A12	a13	c13	A11
A14	a14	c14	A13
A16	a15	c15	A15
A18	a16	c16	A17
CM0	a17	c17	A19
CM2	a18	c18	CM1
ADRSTB*	a19	c19	GND
DATAACK*	a20	c20	DATSTB*
TFRERR*	a21	c21	GND
ATNRQ0*	a22	c22	SYSRST*
ATNRQ2*	a23	c23	ATNRQ1*
nc	a24	c24	ATNRQ3*
nc	a25	c25	nc
GND	a26	c26	nc
nc	a27	c27	nc
nc	a28	c28	nc
STECLK	a29	c29	+VSTBY
-12V	a30	c30	+12V
GND	a31	c31	+5V
GND	a32	c32	GND

PL4. External Power Connector

Phoenix MCV series two part combicon screw terminal connector. Pinout as:



PL2. SVIF1 Development Interface Module Connector

GND	1	2	GND
/RD	3	4	/WR
D0	5	6	D1
D2	7	8	D3
D4	9	10	D5
D6	11	12	D7
A0	13	14	A1
/CS	15	16	/SVINT
nc	17	18	CLK
+5V	19	20	+5V

PL5. ispLSI Programming Connector - DO NOT USE

2mm grid 10-way connector with pinout as:

GND	1	2	ISPSDO
/ISPEN	3	4	ISPMODE
ISPSDI	5	6	ISPSCK
nc	7	8	nc
+5V	9	10	GND

PL6. Parallel I/O and Counter/timer Connector

F + 5	49	50	48	F + 5
F - 12	47	46	46	F + 12
CT0IN	45	44	44	CT1IN
	43	42	42	
FGND	41	40	40	
CT0OUT	39	38	38	CT1OUT
SCU0RX	37	36	36	
SCU0TX	35	34	34	/SCU0CS
	33	32	32	
FGND	31	30	30	
I/O 7	29	28	28	I/O 8
I/O 5	27	26	26	I/O 6
I/O 3	25	24	24	I/O 4
I/O 1	23	22	22	I/O 2
FGND	21	20	20	
IN7	19	18	18	IN8
IN5	17	16	16	IN6
IN3	15	14	14	IN4
IN1	13	12	12	IN2
FGND	11	10	10	ILE
OUT7	9	8	8	OUT8
OUT5	7	6	6	OUT6
OUT3	5	4	4	OUT4
OUT1	3	2	2	OUT2
FGND	1			FGND

Note: During development of the Target188EB it has been found that some manufacturers 50-way IDC connectors foul the PC/104 boards (even with the strain relief removed) when used for the I/O connections. The following connectors have been used with no problems on these boards:

Harting - part no. 0918-550-6813

2E - part no. 517-095-009-050

BERG - part no. 77336-050

There may be others that are satisfactory, but we cannot guarantee that they will fit.

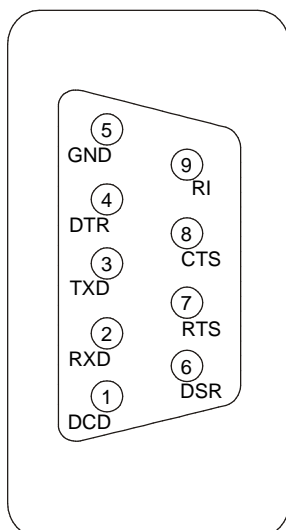
PL7 . PC/104 Connectors

One 64 way non-stackthrough 0.1” grid socket connectors. Pinout and physical arrangement in accordance with PC/104 specification version 2.3.

nc	A1	B1	GND
D7	A2	B2	RESET
D6	A3	B3	+5
D5	A4	B4	nc
D4	A5	B5	nc
D3	A6	B6	nc
D2	A7	B7	-12
D1	A8	B8	ENDXFR*
D0	A9	B9	+12
IOCHRDY	A10	B10	nc
AEN (GND)	A11	B11	SMEMW*
A19	A12	B12	SMEMR*
A18	A13	B13	IOW*
A17	A14	B14	IOR*
A16	A15	B15	pull-up
A15	A16	B16	nc
A14	A17	B17	pull-up
A13	A18	B18	nc
A12	A19	B19	pull-up
A11	A20	B20	SYSCLK
A10	A21	B21	IRQ7
A9	A22	B22	IRQ6
A8	A23	B23	IRQ5
A7	A24	B24	nc
A6	A25	B25	nc
A5	A26	B26	pull-up
A4	A27	B27	nc
A3	A28	B28	BALE
A2	A29	B29	+5
A1	A30	B30	OSC
A0	A31	B31	GND
GND	A32	B32	GND

PL8 and PL9. RS232 Serial Port connectors

Two 9-way D-type plugs. Pinout as:



PL3. Push-button Reset

2 pin Dubox header

GND	1
RST_IN	2

SVIF1 Development Interface Module, PL2

10-way IDC ribbon cable header for use with CAB-SVIF1 in development system.

Channel A TX	1	2	Channel A RX
Channel A RTS	3	4	Channel A CTS
GND	5	6	GND
Channel B CTS	7	8	Channel B RTS
Channel B RX	9	10	Channel B TX

Appendix C. Reference

The STEbus and the TARGET188EB

STEbus is a high reliability 8 bit backplane system, ideal for industrial I/O applications with powerful facilities for multi-processing and interrupt handling.

STEbus boards are classified as either bus masters or slaves. A bus master can initiate a bus transfer whereas a slave can only respond. Generally bus masters are CPU boards which access memory and I/O peripheral slave boards. Some slave boards do have on-board microprocessors.

STEbus master and slave boards may be placed in any slot in the STEbus backplane.

The TARGET188EB can act only as an STEbus master. It may not be used in multi-master systems as it does not have an arbiter necessary to arbitrate between multiple masters.

Only one board in an STEbus system should drive the 16MHz SYSCLK signal.

STEbus slaves are accessed simply by memory and I/O read and write commands from the processor. These generate address strobe (ADRSTB*), data strobe (DATSTB*), command modifier (CM2 to CM0), address and data signals to the STEbus. Slave boards that decode their address for a transfer respond with a DATAACK* signal when they have accepted or placed data on the STEbus. Slave boards should be configured to fit in the STEbus memory or I/O space available on the TARGET188EB. Note that if an STEbus slave has a non-movable address then the memory and I/O maps on the TARGET188EB are very flexible and may be re-configured using registers within the 188EB processor (see memory and I/O maps in Section 4. Using the TARGET188EB).

There are eight interrupt request lines on the STEbus, ATNRQ7* to ATNRQ0*. These are usually driven by slave boards to request action from a master. STEbus interrupt lines are level triggered and slave boards may share interrupt lines. The TARGET188EB can be configured to monitor ATNRQ3*, ATNRQ2*, ATNRQ1* and ATNRQ0*.

All transfers on the STEbus are monitored by bus timeout circuit that terminates any cycles that are longer than 8m. This is required because if no slave board responds to an STEbus cycle then the bus could stay in that bus cycle indefinitely, the bus timeout monitor prevents this. Bus timeouts on the TARGET188EB can optionally (link) generate an interrupt to the 188EB processor to indicate that a transfer problem took place.

PC/104 and the TARGET188EB

PC/104 is a small form factor version of the PC/AT ISA bus (IEEE P996 draft standard) designed for embedded applications. The TARGET188EB is a PC/104 8 bit master controller. It allows 8 bit cycles for both memory and I/O PC/104 peripherals. The TARGET188EB PC/104 interface allows PC/104 expansion boards to extend bus transfers using the IOCHRDY signal and to shorten the default cycle length using ENDXFR*.

The TARGET188EB PC/104 interface supports a subset of the PC/AT interrupts. These are edge triggered.

The TARGET188EB PC/104 interface does not support PC/104 DMA or MASTER* cycles.

There is a PC/104 bus timeout monitor that terminates bus cycles that have been extended to greater than 16us by IOCHRDY.

STEBus and PC/104 interaction on the TARGET188EB

The TARGET188EB can direct expansion bus accesses to either the STEbus or the PC/104 bus. At power-up the PC/104 bus is the default bus. All accesses to addresses not covered by one of the 188EB chip select ranges (see Section 4. Using the TARGET188EB) is directed out onto the PC/104 bus. Four of the 188EB chip select lines are left free for application software to program (GCS7 to GCS4). When one or more of these chip selects is programmed to cover a memory (or I/O) address range then an access to a memory (or I/O) address in that range is automatically re-directed to the STEbus. Using these chip selects then gives the user the ability to mix PC/104 boards and STEbus boards in the address map of the TARGET188EB transparently to the application code.

By using registers within the 188EB processor the address ranges used for the various on-board memory and I/O peripherals can be changed. This means that if the default on-board area of any on-board device conflicts with a device on the STEbus or the PC/104 bus then the chip select that controls that device can be re-programmed.

Programming the 188EB chip selects is fully supported in the C board library supplied with the board.

Appendix D. Bibliography

Intel188EB Embedded Microprocessor Data Sheet
Intel Order No.: 272433-000
Intel188EB Embedded Microprocessor User's Manual
Intel Order No.: 270830-003

These may be ordered from these Intel literature centres:

tel: 1-800-548-4725 U.S. and Canada
tel: 708-296-9333 U.S. (from overseas)
tel: 44(0)1793-431155 Europe (U.K)
tel: 44(0)1792-421333 Germany
tel: 44(0)1793-421777 France
tel: 81(0)120-47-88-32 Japan (fax only)

Or see Intel web site: <http://developer.intel.com/design/intarch/manuals/270830.htm>

IEEE Standard for an 8-bit Backplane Interface: STEbus ANSI/IEEE 1000-1987

The Institute of Electrical and Electronic Engineers Inc.
345 East 47th Street
New York NY 10017
USA
ISBN 1-55937-002-5

PC/104 Specification, Version 2.2

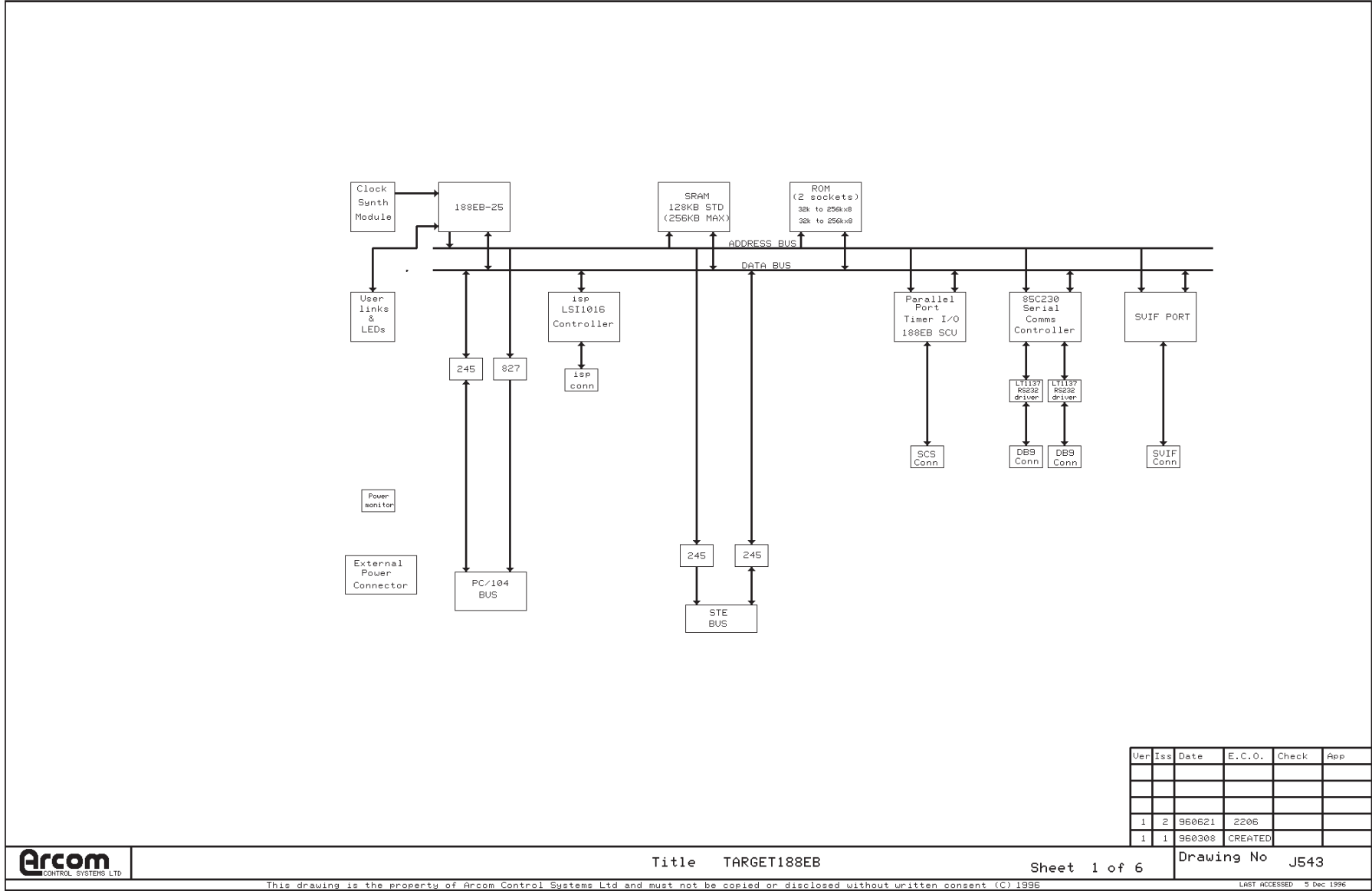
PC/104 Consortium
P.O. Box 4303
Mountain View
CA 94040
USA

tel: 415-903-8304
fax: 415-967-0995

IEEE P996 Draft Standard

IEEE Standards Office
445 Hoes Lane
Piscataway
NJ 08854
USA

Appendix E. Circuit Diagrams



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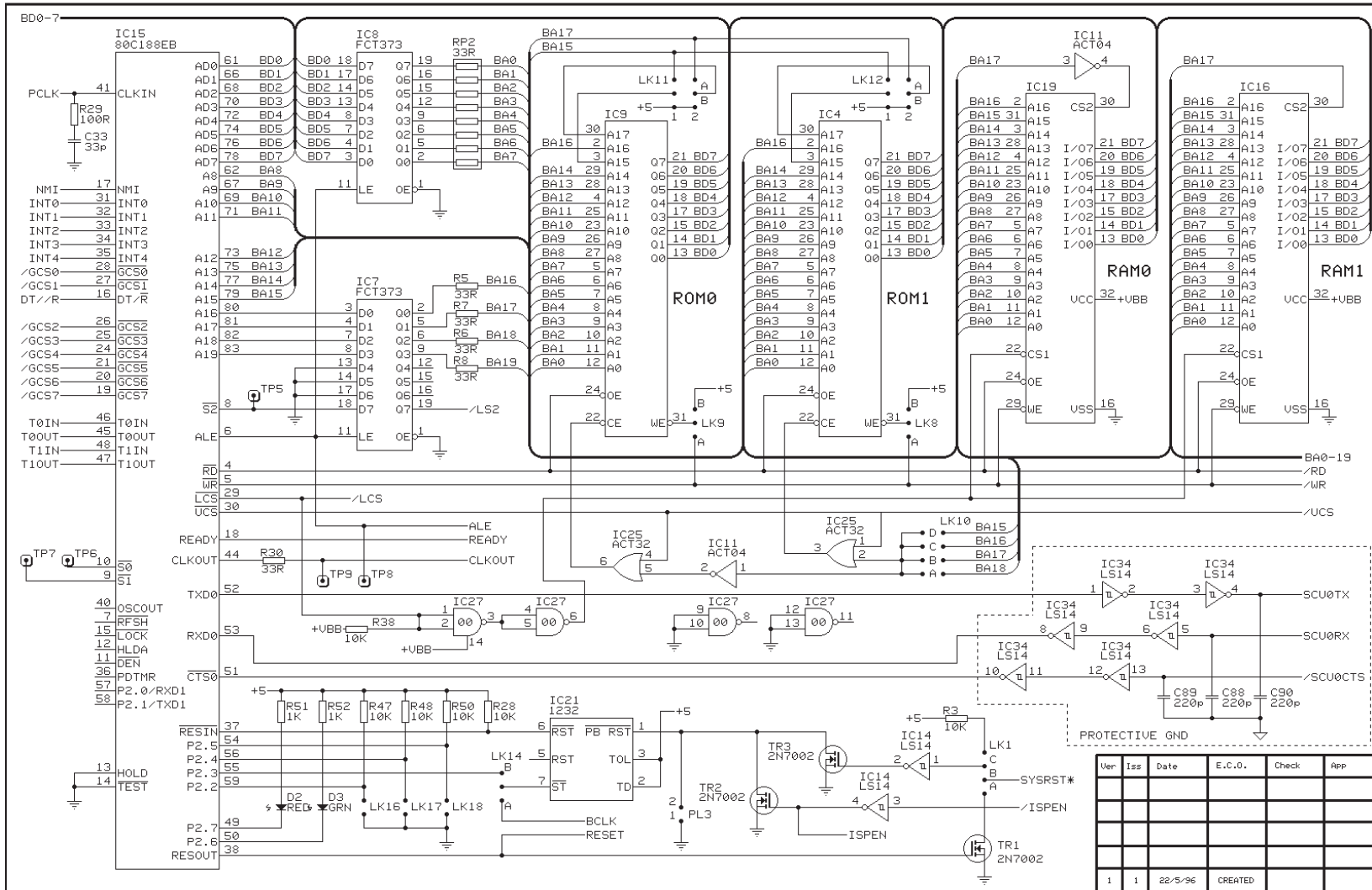
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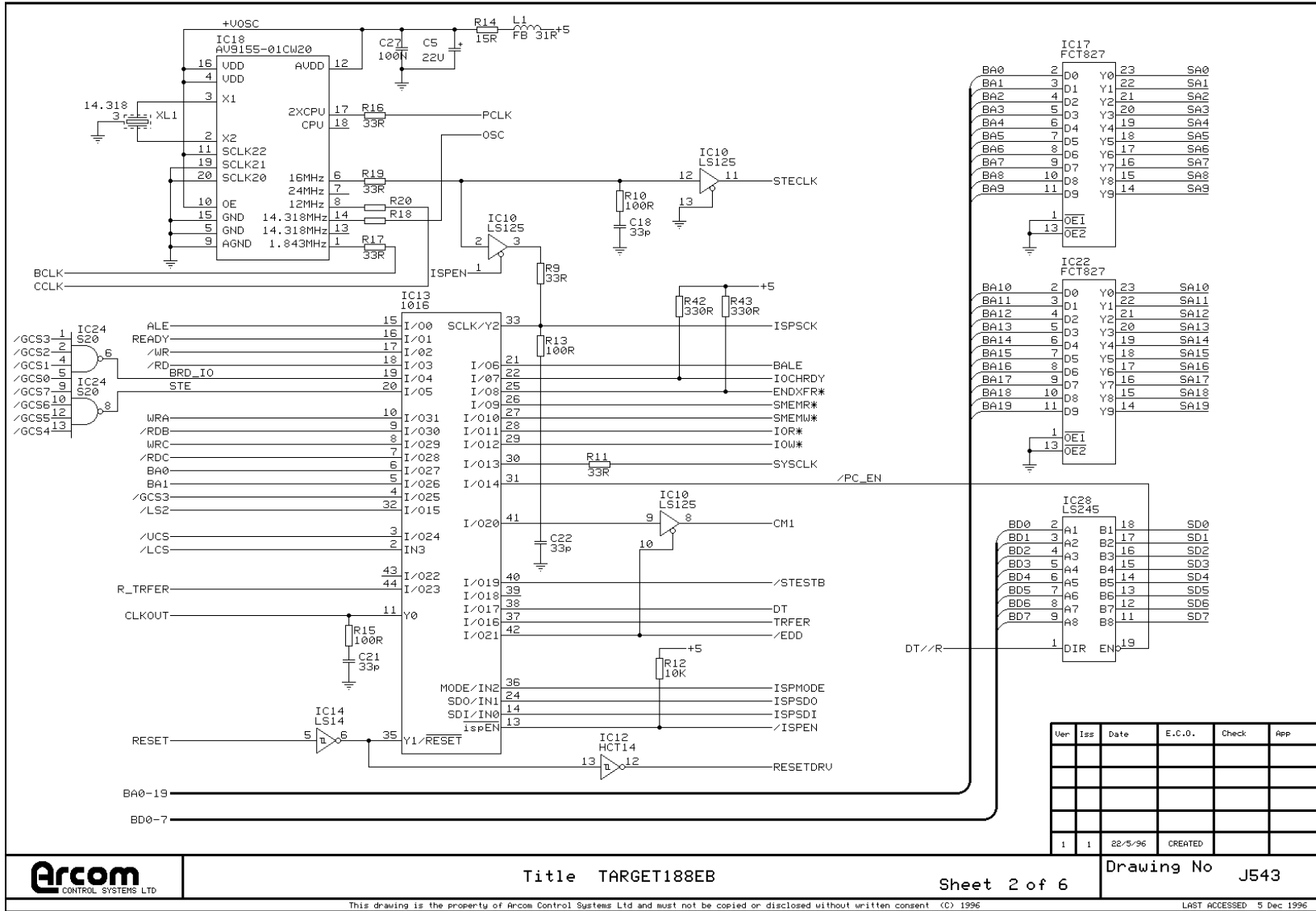
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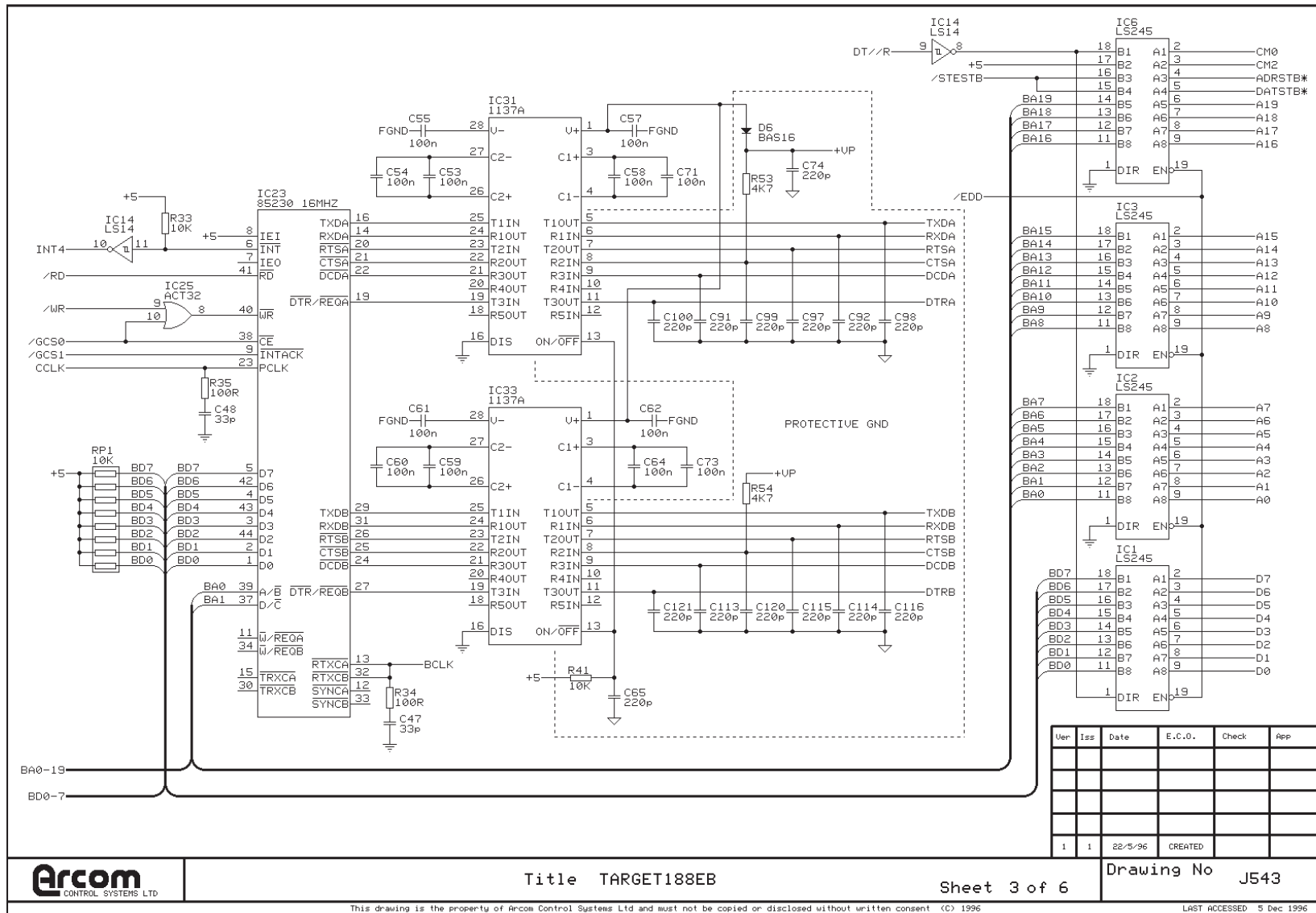


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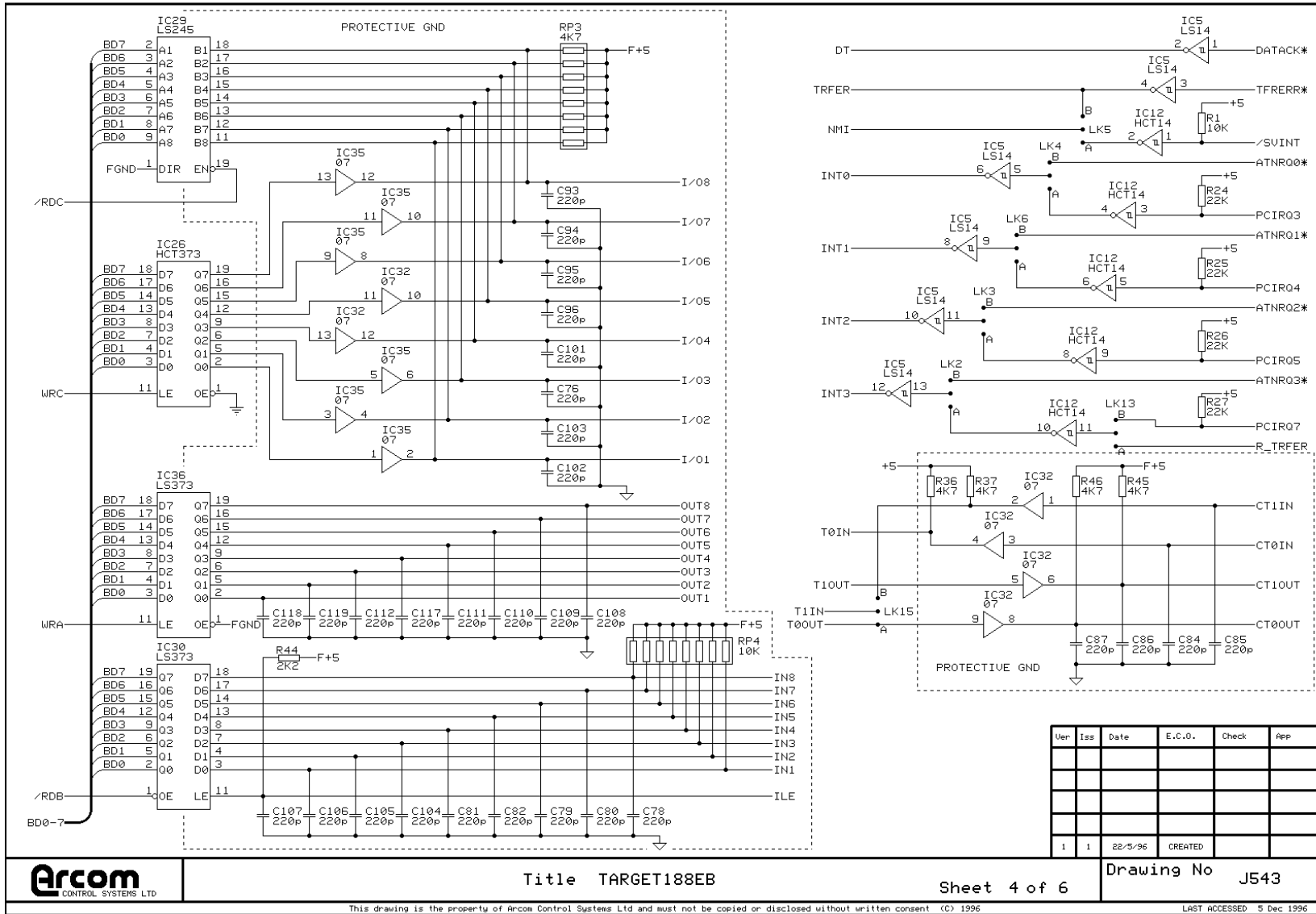
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